AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph [0024] beginning on page 12, as follows:

[0024] A third aspect of the present invention is directed to a method for receiving a transmission frame including a synchronization symbol string, having a synchronization symbol repeated a plurality of times, inserted before a data symbol string. The synchronization symbol is a symbol obtained by synthesizing a plurality of sub band symbols which are orthogonal to each other and having different carrier frequencies. The carrier frequencies of the plurality of sub band symbols are located at an equal predetermined frequency interval. The synchronization symbol includes a synchronization pattern repeated at an interval of a reciprocal of the predetermined frequency interval. The method comprises ~~a step of~~ sampling and analog/digital-converting a transmission frame; obtaining a correlation between the analog/digital-converted signal and the synchronization pattern, and setting the correlation as a synchronization pattern correlation value; detecting a peak of the synchronization pattern correlation value, and setting the peak as a peak timing; detecting a predetermined timing in the synchronization symbol based on the peak timing; detecting a change amount of a phase of the synchronization pattern correlation value in accordance with the predetermined timing and the peak timing, and estimating an error of a frequency of the output from an analog/digital converter based on the change amount of the phase of the synchronization pattern correlation value; obtaining a correlation between each of at least two sub band symbols, among the plurality of sub band symbols, and the signal with the frequency corrected, and setting the correlations as at least two sub band correlations; obtaining a phase difference at a predetermined symbol interval of each of the sub band correlations in accordance with the predetermined timing, and setting the phase difference as an inter-symbol phase difference; estimating an error of the frequency of the output from the analog/digital converter based on the inter-symbol phase difference; setting a phase difference, among the sub bands, of the inter-symbol phase difference in accordance with the predetermined timing as an inter-sub band phase difference; estimating an error of the sampling clock based on the inter-sub band phase difference; correcting the frequency of the analog/digital-converted signal based on the error of the

frequency estimated based on the change amount of the phase of the synchronization pattern correlation value; correcting the frequency of the analog/digital-converted signal based on the error of the frequency estimated based on the inter-symbol pattern phase difference; correcting the frequency of the sampling clock based on the error of the sampling clock estimated based on the inter-sub band phase difference; and demodulating the corrected analog/digital-converted signal.

Please amend the paragraph [0048] beginning on page 25, as follows:

[0048] The timing determination unit 106 determines a predetermined timing at which the synchronization symbol arrives based on the peak timing which is output from the peak detection unit 105. Herein, it is assumed that there are three types of predetermined timing, i.e., a synchronization symbol start timing at which the synchronization symbol is started, a synchronization symbol timing at which the synchronization symbol arrives, and a synchronization symbol termination timing at which the synchronization symbol terminates. When the peak timing is detected at a time interval of the synchronization pattern P a predetermined number of times (d times in the example shown in FIG. 2), the timing determination unit 106 determines that the synchronization symbol string has started and outputs the determination result as the synchronization symbol start timing. When the peak timing stops being detected at the time interval of the synchronization pattern P, the timing determination unit 106 determines that the synchronization symbol string has terminated and outputs the determination result as the synchronization symbol termination timing. The timing determination unit 106 outputs a synchronization symbol timing at the time interval of the synchronization symbol S from the synchronization symbol start timing until the synchronization symbol termination timing.

Please amend the paragraph [0108] beginning on page 45, as follows:

[0108] FIG. 8 shows inter-symbol phase differences of the sub band correlations and inter-sub band phase differences in the case where there are two sub band correlation units. The inter-symbol phase difference detection unit 110 inputs a phase change amount of each sub band correlation (inter-symbol phase difference) to the inter-sub band phase difference detection unit 111 at each synchronization symbol timing. In the case

where there is a clock frequency error, the phase change amount of the sub band correlation which is input from the inter-symbol phase difference detection unit 110 is different between the sub bands. The inter-sub band phase difference detection unit 111 obtains a difference in the phase change amount of the sub band correlation between every two sub bands (inter-sub band phase difference) and averages the obtained inter-sub band phase differences to obtain a clock frequency error. In the example of expression 10, the inter-sub band phase difference detection unit 111 obtains the inter-sub band phase difference between an arbitrary combination of sub bands. More preferably, inter-sub band phase differences are obtained between a plurality of combinations of sub bands and averaged. By obtaining a plurality of phase changes (corresponding to the gradient of the dashed line in the right graph of FIG. 4C) from the inter-sub band phase differences at arbitrary frequency intervals and averaging the phase changes, the influence of noise can be reduced.

Please amend the paragraph [0110] beginning on page 46, as follows:

[0110] The clock generation unit 102 corrects ~~controls~~ the clock frequency based on the held clock frequency error. The A/D converter 101 samples the received signal received after the synchronization symbol termination timing based on the corrected clock frequency.

Please amend the paragraph [0111] beginning on page 46, as follows:

[0111] The data symbol string received after the synchronization symbol termination timing has the carrier frequency error and the clock frequency error corrected, and therefore the demodulation error in the data demodulation unit 112 can be alleviated.

Please amend the paragraph [0128] beginning on page 53, as follows:

[0128] Next, the reception device averages the inter-symbol phase differences obtained so far to obtain a residual frequency error (step S110). The processing in steps S105 through S110 is executed while a second half of the synchronization symbol string is received.